Comchip
SMD Diode Specialist

Introduction to ESD

What is ESD?

Electrostatic Discharge is a high voltage event from the release of electrical energy caused by static electricity or electrostatic induction.

ESD can cause permanent damage to electronics and integrated circuits.

ESD Principle

Protect the IC by suppressing incoming transient voltage to an acceptable level (Output of Vc: Clamping voltage).
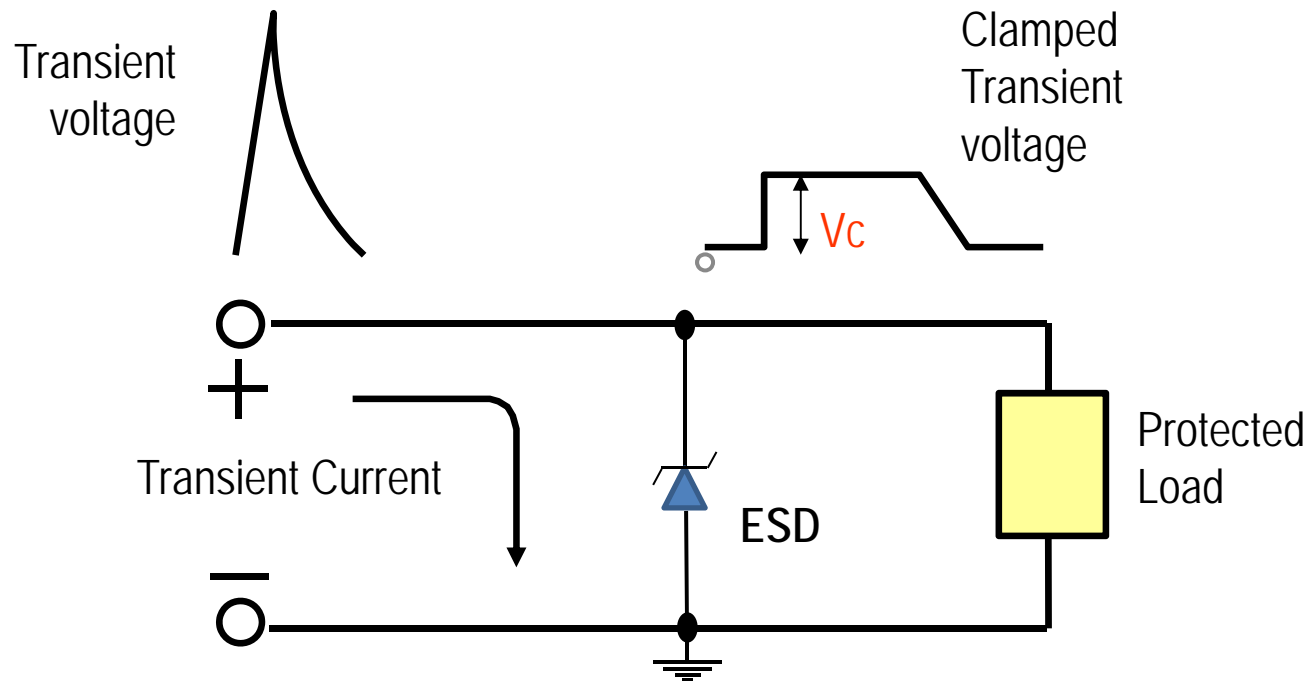
Types of ESD

1) **Sparks** – A spark is triggered when the electric field strength exceeds approximately 4-30kV/cm. This may cause a very rapid increase of free electrons and ions in the air, temporarily causing the air to abruptly become an electrical conductor. eg, lightning.

2) **Corona discharge** – A corona discharge occurs between a highly curved electrode (eg, tip of pen) and an electrode of low curvature (eg flat plate)

3) **Brush discharge** – A brush discharge occurs between an electrode with a curvature between 5mm and 50mm and a voltage of about 500 kV/m. The resulting discharge paths have the shape of a brush.

ESD Simulations

There are three models for assessing the survivability/susceptibility of electronic devices to ESD:

1)Human Body Model, HBM

2)Machine Model, MM

3)Charged Device Model, CDM

Human Body Model - HBM

- Simulates ESD from human contact.

- A person accumulates static electricity from walking or moving and discharges the static through the IC. The leads become the conductive path to a grounded surface due to contact.
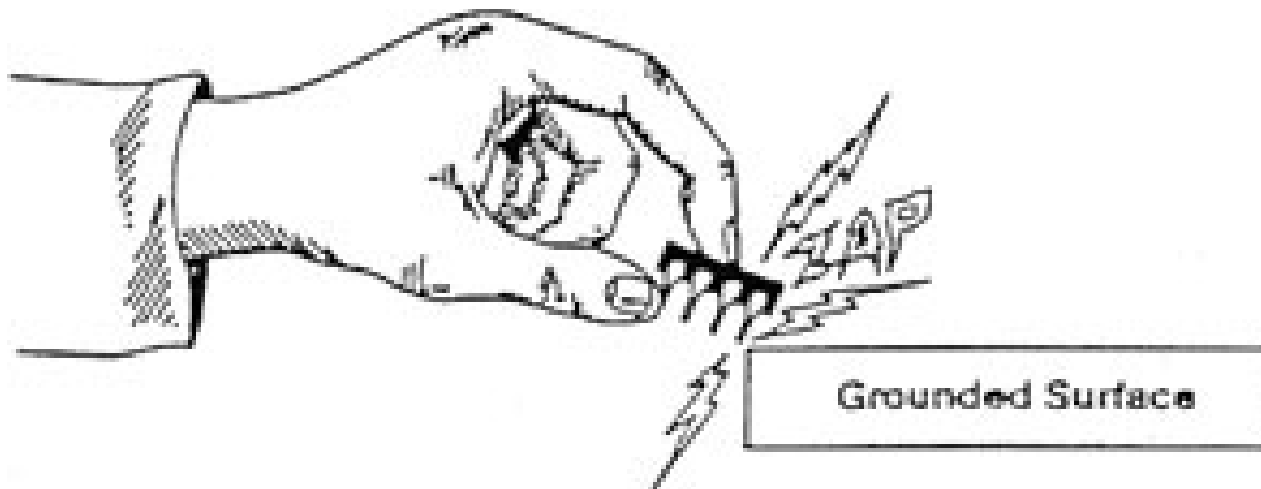
HBM (Human Body Model) test circuit simulates ESD from human contact and consists of 100pF and 1.5KΩ to simulate the equivalent capacitance and resistance of a human body.

The capacitor is charged to a predetermined high voltage from an external source, and then suddenly discharged through the resistor into an electrical terminal of the device under test (DUT).
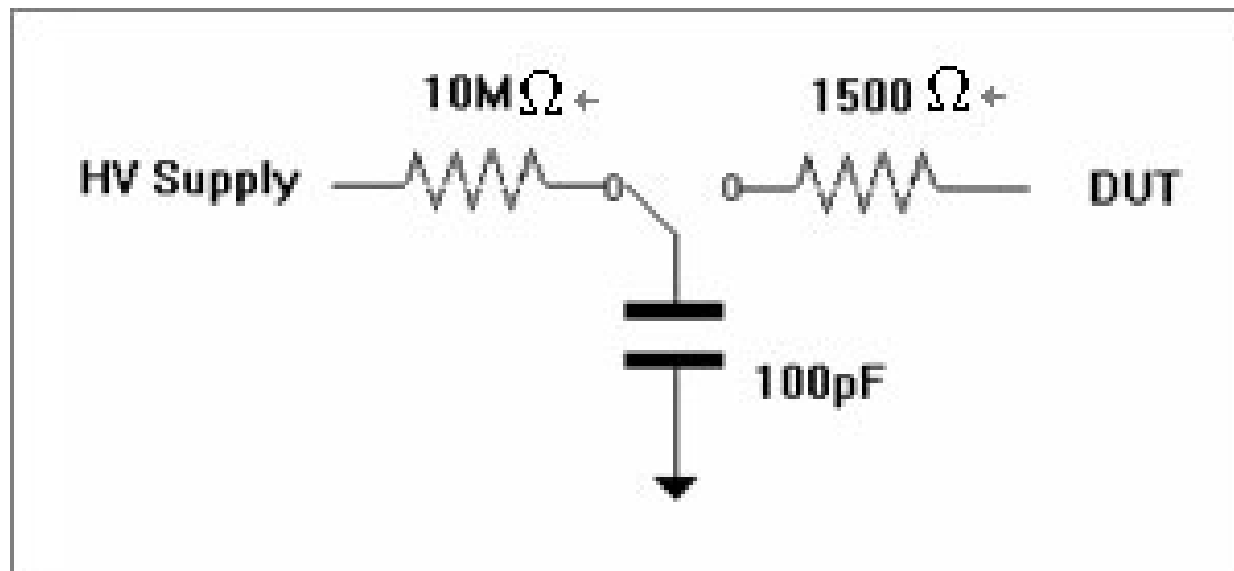

Human Body Model (HBM) test circuit

Machine Model - MM

This simulates the discharge of static electricity accumulated from machines and equipment (i.e. moving mechanical arms, test probes, etc.).

The test circuit consists of charging a 200pF capacitor to a predetermined high voltage from an external source, and then suddenly discharging the DUT through an electrical terminal.
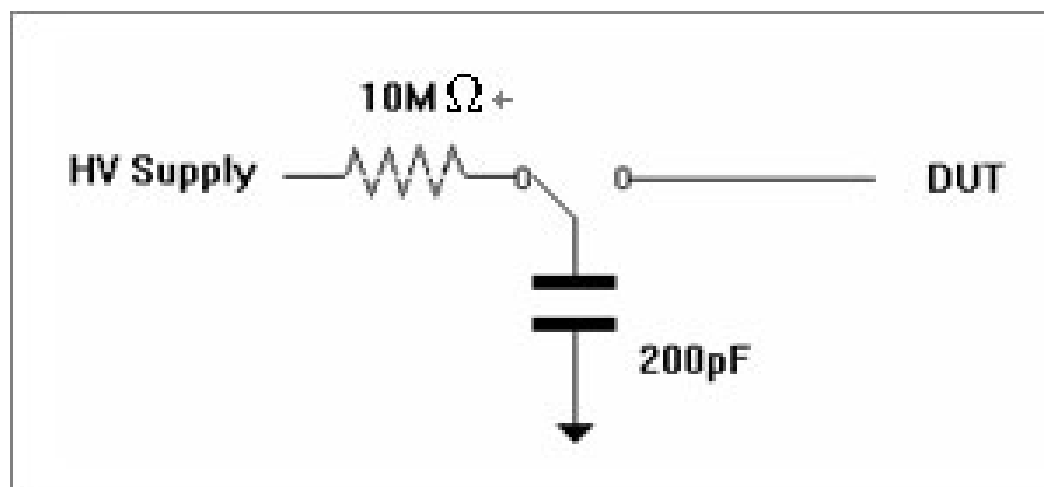

Machine Model (MM) test circuit

Charged Device Model – CDM

The CDM test simulates how the device acts when the device itself has an electrostatic charge and the effects of the discharge when it comes in contact with a metallic surface. This type of discharge is the most common type of ESD in electronic devices and is the main cause of ESD damage during the manufacturing process.

CDM discharge depends mainly on parasitic parameters of the discharge and is strongly dependent on the size and type of component package.

CDM Scenario：

When the IC slides from the packaging tube, friction causes static to form on the device. The IC discharges as the terminals contact a grounded surface (i.e. metal table), or when the part is picked up with metallic tweezers.
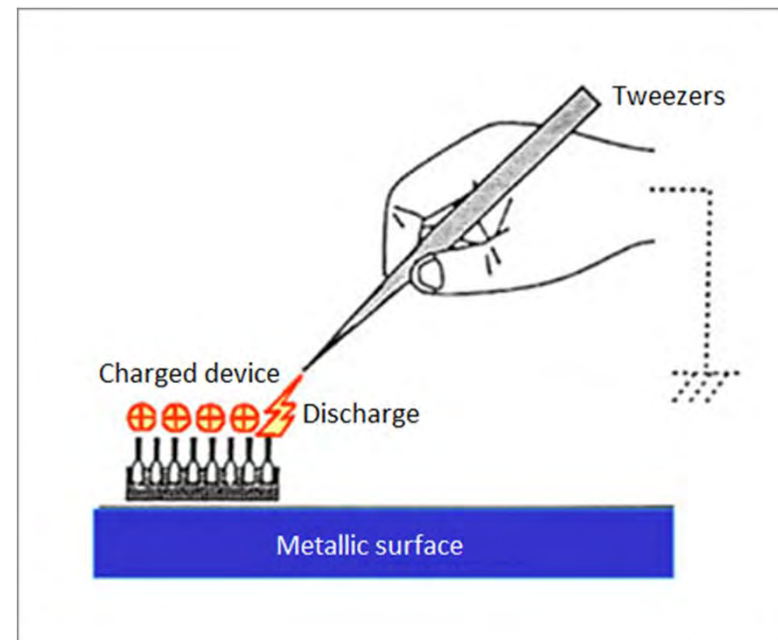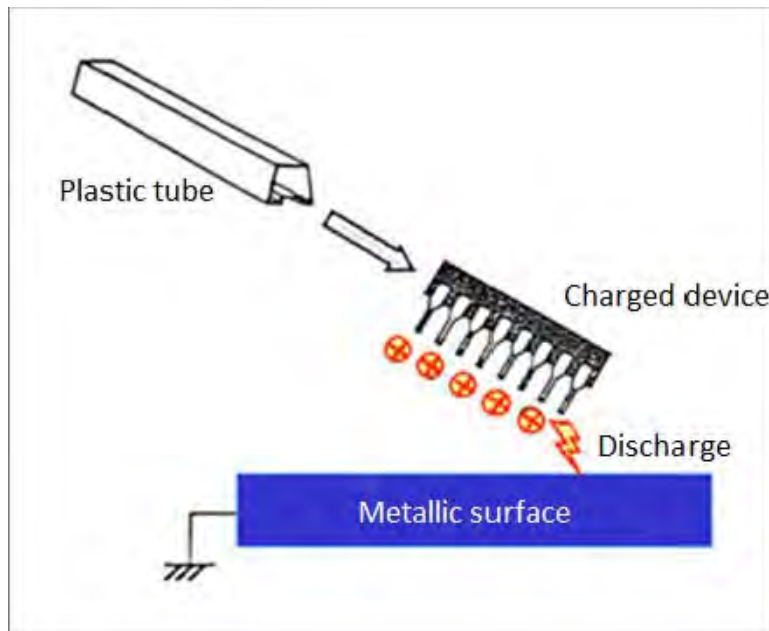
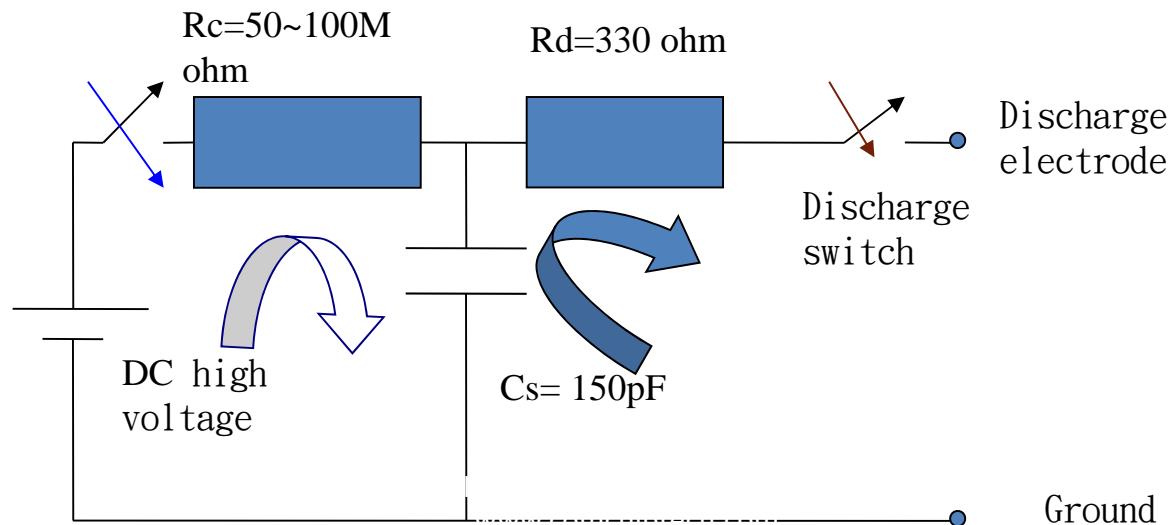# Electrostatic discharge testing (CDM)

Simulates ESD in a charged device at 150pF and 330Ω.

The capacitor is charged to a specific high voltage from an external source, and then suddenly discharged through the resistor into an electrical terminal of the device under test (DUT).

ESD Test circuit

Rc=50~100M ohm

Rd=330 ohm

Discharge electrode

Discharge switch

DC high voltage

Cs= 150pF

Ground

IEC – International Electrotechnical Commission: standards & specifications

61000: Electromagnetic Compatibility (EMC)

Parts 1, 2, & 3: General, Environment, Limits

Part 4: Testing & Measurement Techniques

    4-2: Electrostatic Discharge Immunity

    4-3: Radiated, RF, Electromagnetic Field Immunity

    4-4: Electrical Fast Transients/Burst Immunity

    4-5: Surge Immunity

-IEC61000-4-2 is the series of specifications used to test the susceptibility of electronic devices to ESD.

-Embodies the guidelines and requirements for the test cell geometries, generators, test levels, discharge rate and waveform, types and points of discharge, and functional criteria for gauging product survivability.

-Purpose: to establish a benchmark for testing

-Testing methods and standards are set for Direct Discharge and Air Discharge.

Contact Discharge

Discharge via contact with a conductor.

Preferred test method; more stringent.

Air Discharge

Discharge without direct contact and used only in special circumstances. For example, when the metal (conductive) part of a remote control is covered in insulation.

Contact discharge test

- In the contact discharge test, direct discharges should be applied to all points accessible to the operator during normal use. For example: keyboard controls, display monitor, knobs, power cords, etc.

- Before choosing a discharge point, test susceptible areas 20 times per second, then test selected area using 10 discharges.

Electrostatic discharge test levels

Contact Discharge		Air Discharge	
Level	Voltage/KV	Level	Voltage/KV
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
x	Special	x	Special

Test Result Types

Ratings using standard testing:

[1] Normal performance.

[2] Functionality and performance reduced temporarily but will return to normal.

[3] Functionality and performance are reduced and will require a system reset or repair in order to return to normal.

[4] Equipment failure due to non-reversible capability reduction or loss.
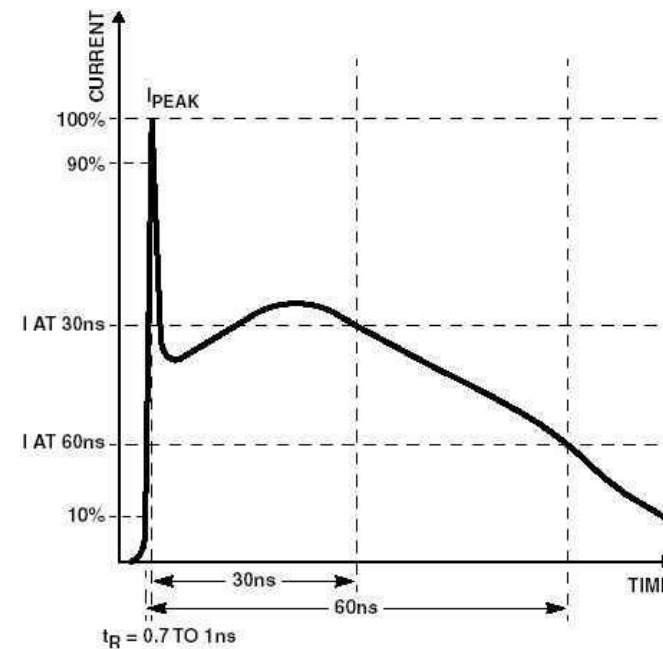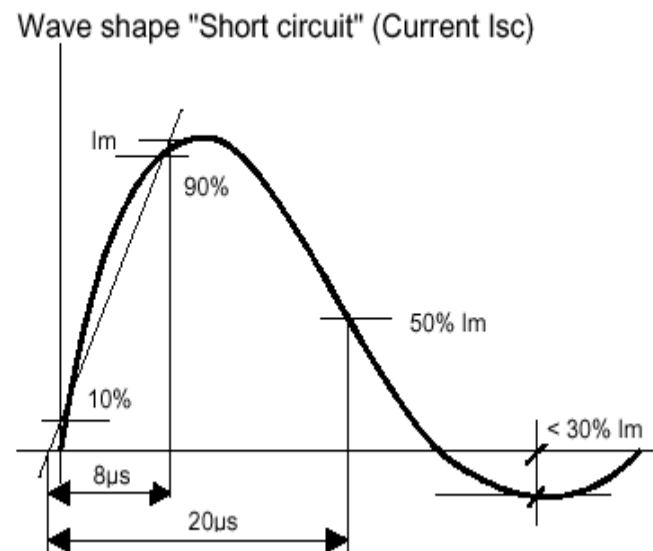
Assessed when: [1]Test passed,[4]Test failed

[2][3]determined by manufacturer and usage type.

Surge and ESD differences

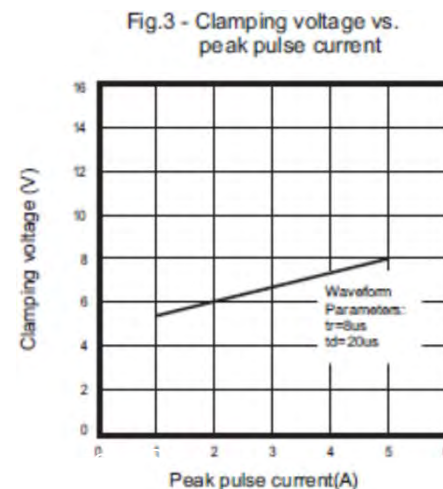|	Surge	ESD
Specifications	IEC61000-4-5	IEC61000-4-2
Features	High-current, low-voltage	High voltage, low current
Energy	Large (Joule)	(Micro-joule)
Time	8×20 or 10×1000uS	0.7~1.0 nS

Input Waveforms

Wave shape "Short circuit" (Current Isc)

ESD Parameters Glossary

Symbol	Parameter
IPP	Pulse Current
VC	Clamping Voltage @IPP
VRWM(VR)	Reverse Voltage
IR(IL)	Maximum Reverse Leakage Current @VRWM
VBR(VBD)	Breakdown Voltage @IT
IT	Test Current
IF	Forward Current
VF	Forward Voltage @IF
PPK(PPP)	Peak Power Dissipation
C(CT)	Max. Capacitance @VR=0 f=1MHz
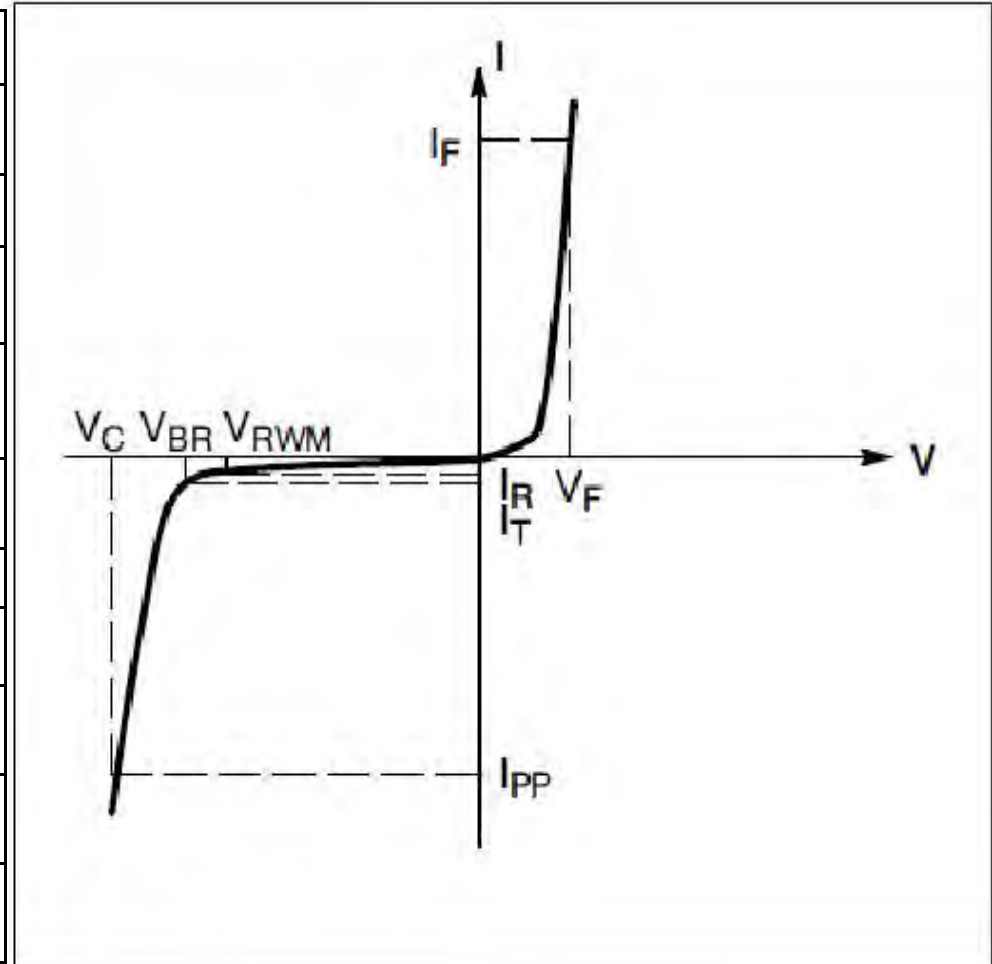
How to choose an ESD Suppressor.

- ESD breakdown voltage (Vbd) has to be **higher** than the circuit requirement.

- ESD Peak Pulse Power (Ppp) has to be **higher** than the maximum surge power of the circuit.

- Multiply Vc by Ipp to calculate Peak Pulse Power (Ppp) using:

    1) Vc & Ipp values in Electrical Characteristics table, or

    2) read from the Vc vs. Ipp curve.

Fig.3 - Clamping voltage vs. peak pulse current

Waveform Parameters: tr=8us td=20us

Clamping voltage (V)

Peak pulse current(A)

How to choose an ESD Suppressor (cont'd)

- Determine ESD device capacitance values (Capacitance): according to the I / O transfer speed.

- Leakage current (Ir): the smaller the better at operating voltage.

- Response time < 1 nS

- Bi-directional ESD is recommended for better protection.

Design recommendations

- Avoid placing sensitive and vital circuits (such as the clock or reset circuits) along the perimeter of the PC board.

- Maximized grounding plane helps to direct ESD away from sensitive components.

- Use shortest trace possible to minimize high frequency interference.

- Multilayer circuit architecture can reduce the ESD impact.

- Place a low-capacitance ESD as close as possible to the protected IC and an ESD as close to the I/O port.

Product Applications

Applications

- Communications → phones, fax, webcams…

- Consumer Electronics → TV, stereo, cell phones…

- Business Machines → photocopying machines, air-conditioners, anti-theft systems…

- Information processing → notebook computers, LCD monitors, modems, scanners, PDAs …

- Industrial machinery → cars, motors, equipment …